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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	4076US (99-01860)
First Inventor or Application Identifier	David E. Charlton
Title	METHOD AND APPARATUS FOR STORING FAILING PART LOCATIONS IN A MODULE
Express Mail Label No.	EL500249729US

jc658 U.S. PTO 04/13/00

jc520 U.S. PTO 09/548026 04/13/00

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents

ADDRESS TO: Assistant Commissioner for Patents
Box Patent Application
Washington, DC 20231

1. [X] * Fee Transmittal Form *(e.g., PTO/SB/17)*
(Submit an original, and a duplicate for fee processing)

2. [X] Specification [Total Pages 13]
(preferred arrangement set forth below)
- Descriptive title of the Invention
- Cross References to Related Applications
- Statement Regarding Fed sponsored R & D
- Reference to Microfiche Appendix
- Background of the Invention
- Brief Summary of the Invention
- Brief Description of the Drawings *(if filed)*
- Detailed Description
- Claim(s)
- Abstract of the Disclosure

3. [X] Drawing(s) *(35 U.S.C. 113)* [Total Sheets 3]

4. Oath or Declaration [Total Pages 2]
a. [X] Newly executed (original or copy)
b. [ ] Copy from a prior application (37 C.F.R. § 1.63(d))
(for continuation/divisional with Box 17 completed)
[Note Box 5 below]
i. [ ] DELETION OF INVENTOR(S)
Signed statement attached deleting inventor(s) named in the prior application, see 37 C.F R. §§ 1.63(d)(2) and 1 33(b).

5 [ ] Incorporation By Reference *(useable if Box 4b is checked)*
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered to be part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

6. [ ] Microfiche Computer Program *(Appendix)*

7. Nucleotide and/or Amino Acid Sequence Submission
(if applicable, all necessary)
a. [ ] Computer Readable Copy
b [ ] Paper Copy (identical to computer copy)
c. [ ] Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. [X] Assignment Papers (cover sheet & document(s))
9. [X] 37 C.F.R.§3.73(b) Statement *(when there is an assignee)* [X] Power of Attorney
10. [ ] English Translation Document *(if applicable)*
11. [X] Information Disclosure Statement (IDS)/PTO-1449 [X] Copies of IDS Citations
12. [ ] Preliminary Amendment
13. [X] Return Receipt Postcard (MPEP 503)
(Should be specifically itemized)
14. [ ] * Small Entity Statement(s) *(PTO/SB/09-12)* [ ] Statement filed in prior application, Status still proper and desired
15 [ ] Certified Copy of Priority Document(s)
(if foreign priority is claimed)
16. [ ] Other. .....

* *A new statement is required to be entitled to pay small entity fees, except where one has been filed in a prior application and is being relied upon.*

17. If a **CONTINUING APPLICATION**, *check appropriate box, and supply the requisite information below and in a preliminary amendment:*
[ ] Continuation [ ] Divisional [ ] Continuation-in-part (CIP) of prior application No _____/_____
Prior application information Examiner _____ *Group / Art Unit* _____

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PATENT
Attorney Docket 4076US (99-01860)

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APPLICATION FOR LETTERS PATENT

for

METHOD AND APPARATUS FOR STORING FAILING PART LOCATIONS IN A MODULE

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METHOD AND APPARATUS FOR STORING FAILING PART LOCATIONS IN A MODULE

BACKGROUND OF THE INVENTION

Field of the Invention: The present invention relates generally to the use of a non-volatile storage device, such as an electrically erasable programmable read only memory device ("EEPROM"), to store information regarding the location of failed parts on a multi-chip module such as a memory module. More particularly, the present invention relates to storing, in an on-module EEPROM, the identities of module output terminals, such as data query ("DQ") terminals which, during testing of the module, have been determined to fail and are thus indicative of the locations of corresponding failed components.

State of the Art: Recent computer memory modules include a non-volatile storage device, such as an electrically erasable programmable read only memory device ("EEPROM"), an erasable programmable read only memory device ("EPROM"), a ferro-electronic device or a flash memory chip, on the memory module with other volatile storage devices such as random access memory ("RAM"), synchronous dynamic random access memory ("SDRAM") and dynamic random access memory ("DRAM"). Volatile storage devices are those memory devices in which information stored in a memory cell in the device is completely lost when the power supply voltage applied to the memory cell is interrupted or turned off. In contrast, information stored in the cells of non-volatile storage devices is preserved when the power supply is turned off. A non-volatile storage device on a memory module is conventionally used to store valuable configuration information necessary for the processor to access the memory on the module. The configuration information stored on the non-volatile storage device include such parameters as the latency and speed of the module components and the size and type of memory module, and are accessed by the processor during initialization of the system. The memory of the EEPROM is divided into sections, each section storing a different category of information.

Typically, however, the capacity of the EEPROM, or other long-term memory storage device, is greater than the memory requirements for the configuration information which needs to be stored. The industry has established a standard of a minimum of 128 bytes as the volume of configuration data to be stored on the non-volatile storage device. Therefore, any EEPROM memory (in excess of 128 bytes) remaining unused may be used to store additional information that is not material to the functionality of the module. The memory capacity of an EEPROM in excess of 128 bytes varies by the capacity of the EEPROM used.

U.S. Patent 5,996,096 to Dell et al. (November 30, 1999), the disclosure of which is hereby incorporated herein by reference, discloses using the excess memory capacity of an EPROM mounted on a memory module to store a map of the bad memory addresses of "reduced specification DRAM chips" (e.g. chips with nonfunctional memory addresses or partially defective DRAM chips) for use during operation of the memory module. According to the invention of Dell et al., a plurality of memory chips or dice are each coded and marked with a unique identifier and tested in accordance with conventional testing methods. Figures 1-3 depict an example of the invention of Dell et al. using a 72 pin single in-line memory module ("SIMM") 2 comprising a printed circuit board ("PCB") 4 having a plurality of electrical contacts 6 (72 in example) along one edge. Those tested memory chips having one or more bad memory cells are identified as "reduced specification chips" 8, 10, 12, 14, 16, 18, 20 and 22 and are placed together on the SIMM 2. Each of the reduced specification chips are identified and their positions recorded using their respective unique identifiers (not shown). The address maps which identify specific bad addresses for each of the chips 8, 10, 12, 14, 16, 18, 20 and 22, are programmed into an EPROM 24 placed on the PCB 4 and associated with each of the respective unique identifiers of the chips 8, 10, 12, 14, 16, 18 and 20. During later testing or operation of the memory module, the address map stored in the EPROM 24 is routinely accessed and updated by system processes to enable a logic device 26, such as an application specific integrated circuit ("ASIC"), or other programmable logic device which contains the bit steering logic and timing generation logic, to redirect the data for

defective DRAM addresses to an alternate storage device for all read and write operations in real time.

Memory Corporation of the United Kingdom sells a dual-in-line-memory-module built with a number of partially defective SDRAM dice. The synchronous dynamic random access memory dice ("SDRAM") used on the dual in-line memory module ("DIMM") are selected to ensure that the total number of defects is within the mapping capabilities of the ASIC. A map of the defective locations is stored in a serial EEPROM mounted on the DIMM. The mapping data is loaded into the ASIC at power-up together with the configuration information to redirect the data for defective DRAM addresses to an alternate storage device.

U.S. Patent 5,963,463 to Rondeau, II et al. (Oct. 5, 1999), the disclosure of which is hereby incorporated herein by reference, also discloses an example a memory module and method employing an EEPROM. According to the method of Rondeau, II et al., an EEPROM is programmed with module information after completion of the memory module assembly.

Memory chip manufacturers conventionally employ chip testing systems to individually test each memory chip. These systems test the operability of each memory chip by writing a value into each memory chell within the chip and then reading the contents of that cell. An example of an individual chip testing system is described in U.S. Patent 5,991,215 to Brunelle (Nov. 23, 1999), the disclosure of which is hereby incorporated herein by reference.

The DRAM dice of memory modules are tested subsequent to connection to the memory module's printed circuit board ("PCB") in addition to testing the individual DRAM dice prior to connection because failures may be caused by connection of the dice to the PCB or by the combination of the particular module components. After module testing, the memory modules are reworked, repaired, scrapped, stripped, repinned, rebuilt onto a module, depopulated or "depopped" (memory chips are removed from a module to re-run through chip testing) or sold as a depop product as is well known to one of ordinary skill in the art. Presently, memory modules are tested one module at a time in a wide range of tests to evaluate such things as speed, margin, voltage ranges, output and

input levels, data patterns, functionality and connectivity of printed circuits, as well as being performance tested by operation in personal computers produced by various manufacturers, etc. To identify which specific DRAMs on a module fail one or more in a series of memory tests, the operator must either closely watch the tester monitor and record the location of a failing DRAM on a display map while the tester is testing the next module, or retest a module identified as having a failed DRAM. Because performance requirements for memory modules are constantly increasing, module testing processes are likewise becoming more complex and, consequently, longer and more expensive. Understandably, the cost of equipment to perform these more complex tests is also increasing. Present module testers may cost anywhere from $1.2-3 million each. Including module handlers, a module tester system may cost anywhere from $1.7-3.5 million.

To help reduce overall cost in these more expensive testers, module tester designers have added the ability to test multiple memory modules in parallel rather than one at a time. An example of such memory module testers are manufactured by Advantest America of Santa Clara, California and Teradyne of Boston Massachusetts. Module testers that can test up to 16 modules at a time are presently in development, though this number and the cost of equipment for testing modules will certainly continue to increase as performance requirements increase.

To illustrate how the testing process may affect the cost of a memory module, consider the following example. A process which could test 16 memory modules in parallel through a 5 minute test would produce 192 modules per hour. Assuming a 25% failure rate, which is not atypical, there would be 48 of the 192 memory modules tested which fail the test process. However, when testing 16 modules at a time in parallel, identifying and marking and failures by watching a test monitor during testing is no longer feasible. The modules identified as failed are therefore retested, one at a time, to identify which parts failed for each module. Due to parallelism, the time it takes to test one module or 16 modules is the same (5 minutes). Therefore, it would take a minimum of 4 hours (48 modules × 5 min./module) to find the defects on the 48 failing modules.

The depreciation cost alone on a $1.7 million module tester system is roughly $39 per hour. Thus, the initial module test cost resulting from the equipment alone is $.20 per module. Contrarily, the cost to retest the 48 failures discovered during the initial test is $3.25 per module, a significant increase over the initial test cost. This results in an average module testing cost before rework of $1.02 per module, five times more expensive than without the retesting. It is thus desirable to have a method of testing memory modules which avoids the costly retesting of the memory modules.

SUMMARY OF THE INVENTION

The present invention addresses the problem of how to avoid the conventional, costly step of retesting memory modules identified as failing during the initial testing of the module by storing the identity of failed module components in a non-volatile memory device such as an EEPROM. Failed module components include such elements as data query ("DQ") terminals and memory bits which require memory mapping of bad addresses. A plurality of memory dice may be placed on a memory module with other module components and the module than tested to identify any failed outputs. The locations of failed component parts, such as memory dice, are determinable from the failed output identifiers which are stored during testing in a non-volatile storage device for access after the testing process. By storing the failed output identities on the memory module itself, locations of specific defective parts may be easily identified and immediately repaired or replaced without the requirement of an additional memory module test, or a requirement of maintaining an association between a particular memory module and its test data. Other module or die information may also be stored on the memory module such as lot identification numbers or other production information, for access at a later time.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

The nature of the present invention as well as other embodiments of the present invention may be more clearly understood by reference to the following detailed

description of the invention, to the appended claims, and to the several drawings herein, wherein:

Figure 1 is a front view of a prior art SIMM DRAM assembly;

Figure 2 is a side view of the prior art SIMM DRAM assembly of Fig. 1;

Figure 3 is a back view of the prior art SIMM DRAM assembly of Fig. 1;

Figure 4 is an illustration of a DIMM DRAM assembly according to the present invention;

Figure 5 is a block diagram of a computer system including non-volatile memory in combination with volatile memory according to the present invention.

DETAILED DESCRIPTION OF THE INVENTION

Figure 4 illustrates a dynamic random access memory ("DRAM") dual in-line memory module ("DIMM") 32. The DIMM 32 shown comprises a printed circuit board ("PCB") 34, or other carrier substrate bearing circuit traces, having a plurality of electrical contacts 36 (numbering 168 in the illustrated example, 84 on each side) along one edge. Each of the electrical contacts 36 are coupled to at least one of a plurality of terminals 37 of functional DRAM 38, 40, 42, 44, 46, 48, 50 and 52, or an EEPROM 54. The DIMM 32 also includes two impedance resistors 55 and 56 and a temporary connection jumper 57.

According to an embodiment of the present invention, a plurality of DRAM dice or chips which have previously been individually tested and determined to be fully functional, or at least functional to an extent usable within a particular application such as partially good die. Additionally, more stringent tests may be performed prior to affixation of a given die to a module to establish that a die is also a "known good die" ("KGD"). The functional DRAM 38, 40, 42, 44, 46, 48, 50 and 52 are then attached, by wire bonding, TAB bonding, flip-chip bonding or other method known in the art, to bond pads (not shown) on the PCB 34 to form the DIMM 32. The DIMM 32 is tested using conventional equipment known in the art such as that previously referenced herein. The identities of any outputs, such as data query ("DQ") terminals, which fail any of the tests in a testing process are detected and recorded in the excess memory of the EEPROM

through programming. The identities of the failed outputs may be recorded either immediately as each fails a test, or at some point subsequent to the test failure, such as at the completion of all tests involving a particular part or at completion of the module test process.

Upon completion of the module test process, unlike prior test methods, if a module is identified as having a failed output, rather than retesting the module to identify the specific module part which failed the test, the portion of the EEPROM storing the identities of the failed outputs may be accessed using methods known in the art, to identify which DRAM, or other module component, needs to be replaced. In this way, the costly retesting step for identifying defective parts on failed modules is unnecessary.

One particular advantage of the present invention is that it may be implemented without costly additional equipment. By modifying the test process software to program the identities of failing outputs into unused portions of the memory in an EEPROM, the advantages of the invention may be achieved. Upon completion of the testing process, any modules which failed the test may then be placed in an inexpensive apparatus as known in the art where the EEPROM may be read for the identities or locations of terminals and a failure map displayed. From the identities of the failing terminals, the corresponding failing part may be identified and marked for repair or replacement. After repair or replacement, the memory module may again be tested and the process repeated until none of the module parts fail a test.

It is contemplated that the process of the present invention will be particularly beneficial to identifying failed DRAM, as the failure rate of DRAM is relatively high. However, as will be clear to one of ordinary skill in the art, the method and apparatus of the present invention may be applied to any testing process where it would be advantageous to have a data record indicative of failed part locations on-board the memory module. It will be understood by those having skill in the technical field of this invention that the invention is applicable to any multi-chip module including a non-volatile storage device including, for example, and without limitation thereto, DRAM SIMMs, DIMMs and Rambus in-line memory modules ("RIMM").

Figure 5 is a block diagram of a computer system 60 which includes a memory module 62 tested according to the present invention comprising a plurality of memory devices and at least one non-volatile storage device 63. The computer system 60 includes a processor 64 for performing various computing functions, such as executing specific software to perform specific calculations or tasks. In addition, the computer system 60 includes one or more input devices 68, such as a keyboard or a mouse, coupled to the processor 64 to allow an operator to interface with the computer system 60. Typically, the computer system 60 also includes one or more output devices 70 coupled to the processor 64, such output devices typically being a printer, a video terminal or a network connection. One or more data storage devices 72 are also typically coupled to the processor 64 to store data or retrieve data from external storage media (not shown). Examples of conventional storage devices 72 include hard and floppy disks, tape cassettes, and compact disks. The processor 64 is also typically coupled to a cache memory 74, which is usually static random access memory ("SRAM") and to the memory module 62.

By using the method and apparatus of the present invention for storing failing part locations in a module, expensive retesting of modules including failed parts may be avoided. Avoiding retesting of failed modules results in a significant cost savings over conventional methods and apparatus requiring such retesting as discussed herein.

Although the present invention has been shown and described with respect to an illustrated embodiment, various additions, deletions and modifications thereto will be apparent to a person of ordinary skill in the art to which the invention pertains and, even if not shown or specifically described herein, are deemed to lie within the scope of the invention as encompassed by the following claims.

CLAIMS

What is claimed is:

1. A memory module comprising:

a plurality of memory devices; and

at least one non-volatile storage device storing data indicating a location of at least one failed part associated with at least one of the plurality of memory devices.

2. The memory module of claim 1, wherein the at least one non-volatile storage device is one of an EEPROM, an EPROM, a ferro-electronic device and a flash memory chip.

3. The memory module of claim 1, wherein the at least one failed part comprises at least one failed output.

4. The memory module of claim 1, wherein at least a portion of the plurality of memory devices are fully functional dice.

5. A computer system comprising:

a processor; and

a memory module comprising:

a plurality of memory devices; and

a non-volatile storage device storing data indicating the location of at least one failed part associated with at least one of the plurality of memory devices.

6. The computer system of claim 5, wherein the at least one non-volatile storage device is at least one of an EEPROM, an EPROM, a ferro-electronic device and a flash memory chip.

7. The computer system of claim 6, wherein the at least one failed part comprises at least one failed output.

8. The method of claim 5, wherein at least a portion of the plurality of memory devices are fully functional dice.

9. A method of testing a memory module, the method comprising:
testing a memory module including a plurality of memory devices thereon;
identifying data indicative of the locations of at least one failed part associated with at least one of the plurality of memory devices; and
storing the data on the memory module.

10. The method of claim 9, wherein storing data of at least one failed part includes storing identification of at least one failed output.

11. The method of claim 9, wherein storing identification of each failed output further comprises storing data in at least one non-volatile storage device on the memory module.

12. The method of claim 11, further comprising selecting the at least one non-volatile storage device from at least one of an EEPROM, an EPROM, a ferro-electronic device and a flash memory chip.

13. The method of claim 9, further comprising accessing the stored data and identifying a location of at least one of the plurality of memory devices including at least one failed part.

14. The method of claim 13, further comprising repairing or replacing memory devices on the memory module identified as having at least one failed part.

15. A method of fabricating a memory module, the method comprising:

placing a plurality of memory devices on a memory module substrate;

testing each of a plurality of elements associated with each of the plurality of memory devices on the memory module; and

storing data indicative of a location of at least one memory device including at least one element which failed a test.

16. The method of claim 15, further comprising subsequently accessing the stored data indicative of a location of at least one memory device including at least one element which failed a test.

17. The method of claim 16, further comprising identifying at least one memory device having at least one failed element and repairing or replacing the at least one identified memory device on the memory module.

18. The method of claim 17, further comprising testing the at least one repaired or replaced memory devices on the memory module.

19. The method of claim 15, wherein storing data indicative of a location of at least one memory device including at least one element which failed a test includes storing data indicative of at least one failed output.

ABSTRACT OF THE DISCLOSURE

A non-volatile storage device on a memory module comprising a plurality of memory devices is used to store the locations of defective parts on the memory module, such as data query ("DQ") terminals, identified during a testing procedure. After testing, the non-volatile storage device, such as an electrically erasable programmable read only memory ("EEPROM"), may be accessed to determine specific memory devices such as dynamic random access memory ("DRAM") which need to be repaired or replaced rather than re-testing the specific memory module.

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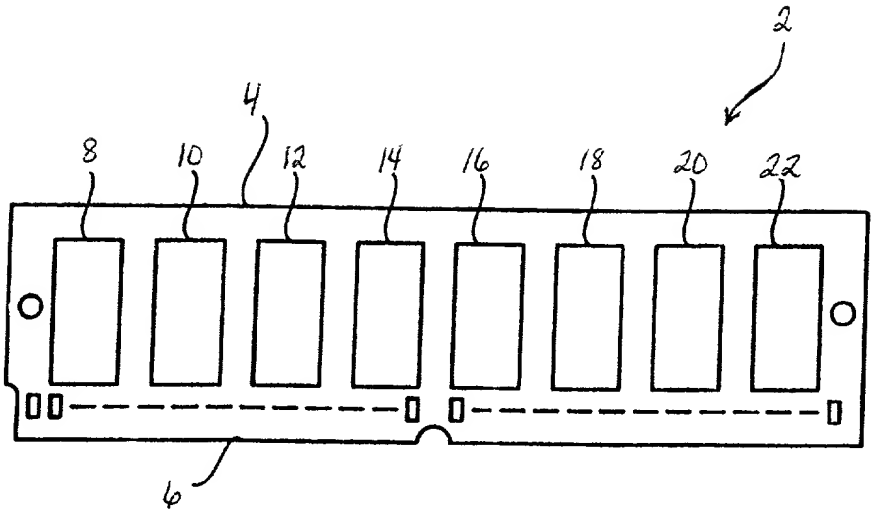


FIG. 1 (PRIOR ART)

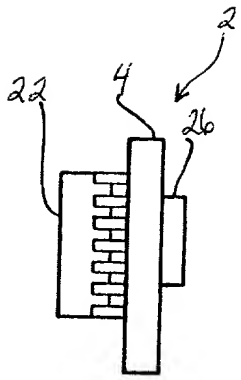


FIG. 2
(PRIOR ART)

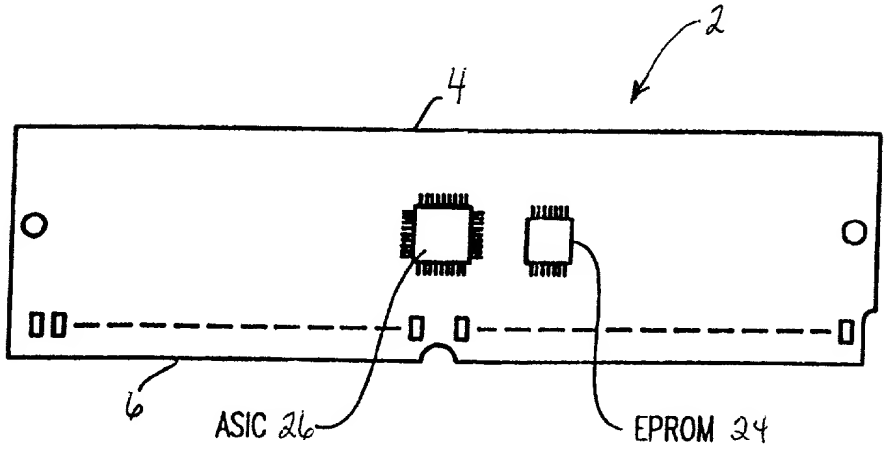
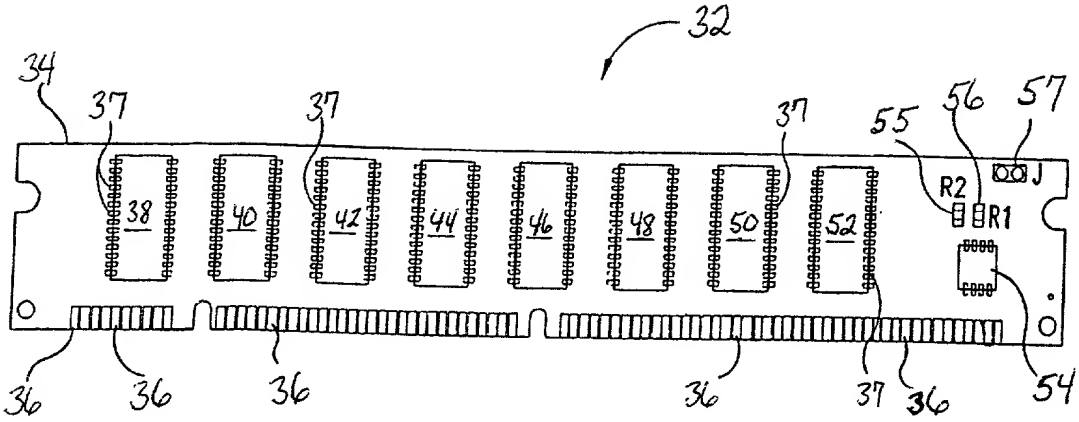


FIG. 3
(PRIOR ART)


32
34
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56
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R2
R1
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Fig. 4

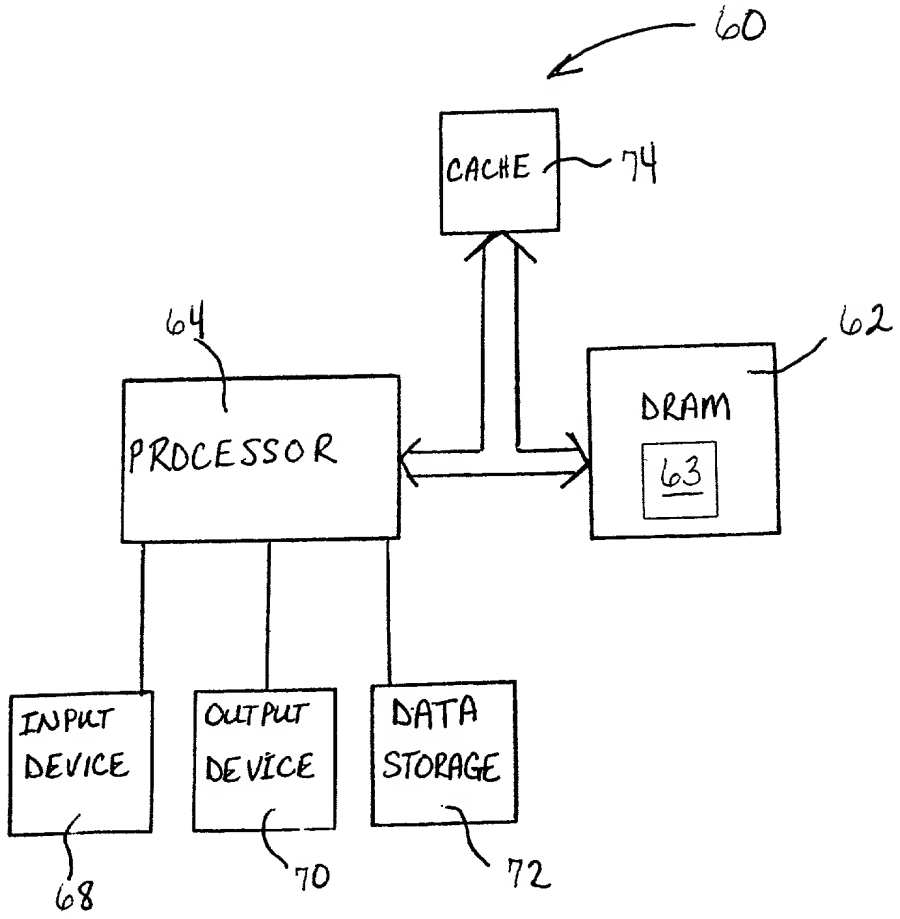
60
CACHE
74
64
62
PROCESSOR
DRAM
63
INPUT DEVICE
OUTPUT DEVICE
DATA STORAGE
68
70
72

Figure 5

DECLARATION FOR PATENT APPLICATION (WITH POWER OF ATTORNEY)

As an inventor named below or on any attached continuation page, I hereby declare that:

My residence, post office address and citizenship are as stated next to my name.

I believe that I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled METHOD AND APPARATUS FOR STORING FAILING PART LOCATIONS IN A MODULE, the specification of which (check one):

- ☒ is attached hereto.
- ☐ was filed on _____ as United States application serial no. _____ and was amended on _____.
- ☐ was filed on _____ as PCT international application no. _____ and was amended under PCT Article 19 on _____.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose to the U.S. Patent and Trademark Office all information known to me to be material to the patentability of the subject matter claimed in this application, as "materiality" is defined in Title 37, Code of Federal Regulations § 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, § 119(a)-(d) or § 365(b) of any foreign application(s) for patent or inventor's certificate or § 365(a) of any PCT international application(s) designating at least one country other than the United States of America listed below and on any attached continuation page and have also identified below and on any attached continuation page any foreign application for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America having a filing date before that of the application(s) on which priority is claimed.

Prior foreign/PCT application(s):

(number)	(country)	(day/month/year filed)	Priority Claimed Yes	No
(number)	(country)	(day/month/year filed)	Yes	No

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) or § 365(c) of PCT international application(s) designating the United States of America listed below and on any attached continuation page and, insofar as the subject matter of each of the claims of this application is not disclosed in any such prior application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose to the U.S. Patent and Trademark Office all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations § 1.56 which became available between the filing date of such prior application and the national or PCT international filing date of this application:

(application serial no.)	(filing date)	(status - pending, patented or abandoned)
(application serial no.)	(filing date)	(status - pending, patented or abandoned)

I hereby claim the benefit under Title 35, United States Code, § 119(e) of any United States provisional application(s) listed below:

(provisional application no.)	(filing date)

I hereby appoint the following Registered Practitioners to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith:

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P.O. BOX 2550
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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of first joint inventor: David E. Charlton
Inventor's signature David E Charlton Date March 14, 2000
Residence: Star, Idaho
Citizenship: U.S.A.
Post Office Address: 4095 Pollard Lane, Star, ID 83669

DECLARATION FOR PATENT APPLICATION
(continuation page)

Invention title: METHOD AND APPARATUS FOR STORING FAILING PART LOCATIONS IN A MODULE

Inventor name(s) appearing on first declaration page: David E. Charlton

☒ Additional original, first and joint inventor(s):

Full name of second joint inventor: Sovandy N. Prak
Inventor's signature Sovandy N. Prak Date 04-02-00
Residence: Meridian, Idaho
Citizenship: U.S.A.
Post Office Address: 4230 E. Venture Place, Meridian, ID 83642

Full name of third joint inventor: Keith E. Robinson
Inventor's signature Keith E. Robinson Date 3-14-00
Residence: Caldwell, Idaho
Citizenship: U.S.A.
Post Office Address: 2011 Terrace Drive, Caldwell, ID 83605

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Charlton et al.	**Examiner:**	Unknown
Serial No.:	Not Yet Assigned	**Group Art Unit:**	Unknown
Filed:		**Attorney Docket No.:**	4076US (99-01860)
Title:	METHOD AND APPARATUS FOR STORING FAILING PART LOCATIONS IN A MODULE		

POWER OF ATTORNEY BY ASSIGNEE AND CERTIFICATE UNDER 37 CFR § 3.73(b)

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

MICRON ELECTRONICS, INC., assignee of the entire right, title and interest by assignment from the inventor(s) in the above-identified application, hereby appoints the following attorneys and agents:

David V. Trask, Reg. No. 22,012	William S. Britt, Reg. No. 20,969	Thomas J. Rossa, Reg. No. 26,799
Laurence B. Bond, Reg. No. 30,549	Joseph A. Walkowski, Reg. No. 28,765	James R. Duzan, Reg. No. 28,393
Allen C. Turner, Reg. No. 33,041	Kent S. Burningham, Reg. No. 30,453	Edgar R. Cataxinos, Reg. No. 39,931
Stephen R. Christian, Reg. No. 32,687	Brick G. Power, Reg. No. 38,581	Kenneth B. Ludwig, Reg. No. 42,814
Paul C. Oestreich, Reg. No. 44,983	Devin R. Jensen, Reg. No. 44,805	David L. Stott, Reg. No. 43,937
Kenneth C. Booth, Reg. No. 42,342	Samuel E. Webb, Reg. No. 44,394	Eleanor V. Goodall, Reg. No. 35,162
Kerry D. Tweet, Reg. No. P-45,959	Hoyt A. Fleming, Reg. No. 41,072	Steven P. Arnold, Reg. No. 33,354
Paul A. Revis, Reg. No. 45,040		

as its attorneys with full power of substitution to prosecute this application and all applications claiming filing date priority therefrom and to transact all business in the U.S. Patent and Trademark Office in connection therewith.

The above-identified assignee hereby elects, pursuant to 37 C.F.R. § 3.71, to conduct the prosecution of the above-identified patent application to the exclusion of the inventor(s).

A chain of title from the inventor(s) of the above-identified patent application to the above-identified assignee is shown:

[] In an assignment recorded in the U.S. Patent and Trademark Office at Reel , Frame .

[X] In an assignment filed herewith for recordation, a true copy of which is attached hereto.

The undersigned has reviewed the above-identified assignment and, to the best of his knowledge and belief, title is in the above-identified assignee.

The undersigned further avers that he is empowered to make and sign the foregoing certification on behalf of the above-identified assignee, and to take the action set forth herein on its behalf.

Please direct all communications regarding the above-identified application to:

Joseph A. Walkowski,
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Salt Lake City, UT 84110
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Respectfully Submitted,

MICRON ELECTRONICS, INC.

Date: 4/10/0

By: _____
Paul A. Revis
Reg. No. 45,040
Intellectual Property Counsel
MICRON ELECTRONICS, INC.

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